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2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,010	CHUNG ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-15 and 17-21* is/are rejected.

7)☒ Claim(s) *7 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20071109*.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21, as amended on 9/20/2007, are pending in the instant application. Applicant's arguments submitted 9/20/2007 have been carefully and fully considered, but are not found persuasive. The new grounds of rejection presented in the instant Office action have been necessitated by amendment. Accordingly, this Office action is made **FINAL**.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claims 2, 12, 18, and 20** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

4. **Claims 2 and 12** recite the limitation "*wherein the meta-information is written after the data of the logical block is written.*"

5. **Claim 20** recites the limitation "*wherein the meta-information is written in the spare area after the data of the logical block is written in the main area*".

6. The Examiner is not aware of a portion of the specification which teaches how the meta-information is written after the data of the logical block is written. Accordingly, one of ordinary skill in the art would not know how to make or use the invention as recited in claims 2, 12, and 20.

7. Claim 18 recites the limitations "*a first write operation which writes the data and the meta-information in a first physical block corresponding to the logical block number, if the first write operation has not previously been performed for the logical block number, and changes the flash memory state information*" and "*a second write operation which writes the data and the meta-information of a second physical block, if the first write operation has been performed for the logical block with the logical block number, wherein the flash memory state information is not changed*". Claim 18 also recites the limitation "*Wherein each physical block of the plurality of physical blocks comprises a logical block number and flash memory state information comprising data and meta-information*". If the recited "flash memory state information" is interpreted as the region of the memory block in which the data representing the flash memory state information is stored, the Examiner can see how the first write operation changes the flash memory state information. Under this interpretation, however, it is unclear from the specification how the second write operation would write data and meta-data of the block would without changing the flash memory state information, as the "flash memory state information" would refer to the physical region where the data is written. If the recited "flash memory state information" is interpreted as the data stored in the previous physical block which indicates the state of the logical block, the Examiner can see how

the second write operation would write data and meta-data of the block would without changing the flash memory state information, but it becomes unclear how the first write operation could change the flash memory state information, as there has not been a write for the logical block and accordingly there would not be any previously written flash memory state information to change. As such, it does not appear that the specification teaches how one would make or use the invention recited in claims 18-21.

8. **Claims 19-21** depend from claim 18, and are rejected for the same reasons as claim 18.

9. **Claims 18-21** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

10. **Claim 18** recites the limitation "*a first write operation which writes the data and the meta-information in a first physical block corresponding to the logical block number, if the first write operation has not previously been performed for the logical block number, and changes the flash memory state information*". The Examiner is not aware of a portion of the specification that teaches that if a first write operation has not been previously been performed for the logical block, the controller changes the flash memory state information. It would seem that if there has not been a first write, there would be no flash memory state information to change.

11. **Claims 19-21** depend from claim 18, and are rejected for the same reasons as claim 18.

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. **Claims 18-21** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

14. **Claim 18** recites the limitation "the flash memory state information" in lines 10-11 and line 14. Claim 18 refers to a plurality of physical blocks, each of which contains flash memory state information. Which flash memory state information recited in lines 10-11 and line 14 is the "the flash memory state information".

15. **Claims 19-21** depend from claim 18, and are rejected for the same reasons as claim 18.

Claim Rejections - 35 USC § 102

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

17. **Claims 1, 3-4, 11, 13-14, 18-19, and 21** are rejected under 35 U.S.C. 102(b) as being anticipated by Conley (US 2002/0099904).

18. **Claim 1** is taught by Conley as:

a. *A flash memory access apparatus, comprising: a flash memory comprising a plurality of units, each of the units comprising a plurality of blocks, and a flash memory controller.* Paragraph 0038 teaches the architecture of a typical non-volatile data storage system, which includes a controller and a plurality of flash memory devices. Paragraph 0040 explains that flash memory cells are divided into multiple pages.

b. *Wherein if a write operation is requested for a logical block number of the flash memory, the flash memory controller is configured to write data and meta-information in a physical block corresponding to a logical block with the logical block number if a previous write operation has not been performed for the logical block.* Paragraph 0062 discusses a method of programming a non-volatile memory. If there are pages in the physical block that have not been written to, the data is written to those blocks.

c. *And the flash memory controller is configured to perform a write operation for writing the data and the meta-information allocated to the logical block in a new physical block without changing flash memory state information written in a previous physical block corresponding to the logical block if the previous write operation has been performed for the logical block.* Paragraph 0049 shows that

when new data is to be written to a logical block corresponding to physical block PBN 0, item 35 of figure 8, which is full, a new physical block PBN 1, item 39 of figure 8, is selected and the new pages are written to PBN 1. Paragraph 0055 shows that an individual page contains data, item 45 of figure 10, and meta-information, item 49 of figure 10. Paragraph 0048 shows that when new pages are written to a logical block, the pages containing the original data are not tagged. The last sentence of paragraph 0047 further emphasizes this by stating "*the writing of the old/new or other flags, as described with respect to FIGS. 6, 7A and 7B, cannot be tolerated.*"

d. *And wherein the flash memory state information is time independent.* Paragraph 0051 shows that the output of a modulo-N counter can be used to generate the value of field 43, which is shown in paragraph 0052 to be used to determine if a block is the most recent block.

19. **Claim 3** is taught by Conley as:

e. *The apparatus as claimed in claim 1, wherein the data and meta-information of the logical block are simultaneously written.* Paragraph 0055 shows that the data 45 and meta-information 49 are part of the same page. As the data and meta-information are part of the same page they would inherently be written simultaneously, as the system of Conley writes data on a page basis.

20. **Claim 4** is taught by Conley as:

f. *The apparatus as claimed in claim 1, wherein the meta-information comprises the logical block number.* Paragraph 0055 shows that overhead data, item 49 of figure 10, contains the logical block number.

g. *And the flash memory state information indicating a state of the physical block as valid, deleted, or invalid.* Paragraph 0055 shows a page contains a time stamp 43, paragraph 0051 shows that the timestamp can be replaced with the output of a modulo-N counter. Paragraph 0050 shows that the time stamp indicates the time the page was written relative to other pages with the same logical address. As shown in paragraph 0052, the time stamps of blocks having the same logical block address and page offset are compared, which allows the system to determine which page is the last written page. Accordingly, this shows what pages are valid.

21. **Claim 11** is taught by Conley as:

h. *A flash memory access method, comprising: accessing the flash memory and searching for a currently writable physical block if a processor requests a write operation for a specific logical block number of the flash memory.* Paragraph 0062 shows that when a write is performed, an available physical page is found.

i. *And writing data and meta-information in a physical block corresponding to a logical block with the logical block number if a previous write operation has not been performed for the logical block.* Paragraph 0062 discusses a method of

programming a non-volatile memory. If there are pages in the physical block that have not been written to, the data is written to those blocks.

j. *And writing the data and the meta-information in a new physical block corresponding to the logical block without changing flash memory state information written in a previous physical block corresponding to the logical block if the previous write operation has been performed for the logical block.* Paragraph 0049 shows that when new data is to be written to a logical block corresponding to physical block PBN 0, item 35 of figure 8, which is full, a new physical block PBN 1, item 39 of figure 8, is selected and the new pages are written to PBN 1. Paragraph 0055 shows that an individual page contains data, item 45 of figure 10, and meta-information, item 49 of figure 10. Paragraph 0048 shows that when new pages are written to a logical block, the pages containing the original data are not tagged. The last sentence of paragraph 0047 further emphasizes this by stating "*the writing of the old/new or other flags, as described with respect to FIGS. 6, 7A and 7B, cannot be tolerated.*"

k. *Wherein the flash memory state information is time independent.* Paragraph 0051 shows that the output of a modulo-N counter can be used to generate the value of field 43, which is shown in paragraph 0052 to be used to determine if a block is the most recent block.

22. **Claim 13** is taught by Conley as:

l. *The apparatus as claimed in claim 11, wherein the data and meta-information of the logical block are simultaneously written.* Paragraph 0055 shows that the data 45 and meta-information 49 are part of the same page. As the data and meta-information are part of the same page they would inherently be written simultaneously, as the system of Conley writes data on a page basis.

23. **Claim 14** is taught by Conley as:

m. *The method as claimed in claim 11, wherein the meta-information comprises the logical block number.* Paragraph 0055 shows that overhead data, item 49 of figure 10, contains the logical block number.

n. *And the flash memory state information indicating a state of the physical block as valid, deleted, or invalid.* Paragraph 0055 shows a page contains a time stamp, paragraph 0051 shows that the timestamp can be replaced with the output of a modulo-N counter. Paragraph 0050 shows that the time stamp indicates the time the page was written relative to other pages with the same logical address. As shown in paragraph 0052, the time stamps of blocks having the same logical block address and page offset are compared, which allows the system to determine which page is the last written page. Accordingly, this shows what pages are valid.

24. The Examiner notes that the rejection of claims 18-19 and 21 are made in light of the rejection of said claims under 35 USC 112 first and second paragraph presented supra.

25. **Claim 18** is taught by Conley as:

o. *A flash memory access apparatus, comprising: a flash memory comprising a plurality of physical blocks.* Paragraph 0038 teaches the architecture of a typical non-volatile data storage system, which includes a controller and a plurality of flash memory devices. Paragraph 0040 explains that flash memory cells are divided into multiple pages.

p. *Wherein each physical block of the plurality of physical blocks comprises a logical block number and flash memory state information comprising data and meta-information.* Paragraph 0055 shows that each page contains an overhead data area 49, which includes the LBN and page tag 41 and time stamp 43, which is used to determine if the stored data is the valid data for the corresponding logical page.

q. *Wherein the flash memory state information is time independent.* Paragraph 0051 shows that instead of a timestamp, a modulo-N counter may be used which is incremented each time a logical block is updated.

r. *And a flash memory controller, wherein if a write operation is requested for the logical block number, the flash memory controller performs one of (a) a first write operation which writes the data and the meta-information in a first physical*

block corresponding to the logical block number, if the first write operation has not previously been performed for the logical block number, and changes the flash memory state information. Paragraph 0055 shows that each page contains overhead data 49. It is inherent that this data is written to the page when the first write is performed for the logical page number, as otherwise the system would be unable to tell if later written data is later or earlier.

s. *And (b) a second write operation which writes the data and the meta-information of a second physical block, if the first write operation has been performed for the logical block with the logical block number, wherein the flash memory state information is not changed.* Paragraph 0049 shows that when new data is to be written to a logical block corresponding to physical block PBN 0, item 35 of figure 8, which is full, a new physical block PBN 1, item 39 of figure 8, is selected and the new pages are written to PBN 1. Paragraph 0055 shows that an individual page contains data, item 45 of figure 10, and meta-information, item 49 of figure 10. Paragraph 0048 shows that when new pages are written to a logical block, the pages containing the original data are not tagged. The last sentence of paragraph 0047 further emphasizes this by stating "*the writing of the old/new or other flags, as described with respect to FIGS. 6, 7A and 7B, cannot be tolerated.*"

26. **Claim 19** is taught by Conley as:

t. *The apparatus as claimed in claim 18, wherein each physical block comprises further comprises a main area which stores the data and a spare area which stores the meta-information, the logical block number and the flash memory state information*. Figure 10 shows that each page contains user data area 45 and overhead area 49.

27. **Claim 21** is taught by Conley as:

u. *The apparatus as claimed in claim 19, wherein the meta-information is written in the spare area simultaneously as the data of the logical block is written in the main area*. Paragraph 0055 shows that the data 45 and meta-information 49 are part of the same page. As the data and meta-information are part of the same page they would inherently be written simultaneously, as the system of Conley writes data on a page basis.

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. **Claims 5-6, 8-10, 15, and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Conley (cited *supra*) in view of Kim et al. (US 6,381, 176).

30. **Claim 5** is taught by Conley as shown *supra* with respect to claim 1.

31. Although Conley teaches that blocks having the same logical block number can be distinguished by their timestamps, it does not disclose expressly performing a recovery operation.

32. With respect to claim 5, Kim teaches:

v. *The apparatus as claimed in claim 1, wherein the flash memory controller is configured to perform a recovery operation which detects, during a scanning process, physical blocks for the logical block number and recovers from an error by determining a valid block for the logical block among the detected physical blocks.* Kim teaches at column 6 lines 29-36 that a recovery operation is required if two valid blocks having the same logical block number exist. In the system disclosed by Conley, paragraph 0050 shows that it can be determined which of multiple pages having the same logical block number and page offset is the correct page by comparing the timestamps of the blocks.

33. At the time of the invention it would have been obvious to one of ordinary skill in the art that a recovery operation is necessary in the event of an error during writing.

34. Conley and Kim are analogous art because they are from the same field of endeavor, the design of flash memory systems.

35. The motivation for doing so would have been to determine which block will be erased during a recovery operation (Kim, column 6 lines 30-36)

36. Therefore, it would have been obvious to combine Kim with Conley for the benefit of determining which pages are old and can be deleted to obtain the invention as specified in **claims 5, 6, and 8-10**.

37. **Claim 6** is taught by Conley as:

w. *The apparatus as claimed in claim 5, wherein the scanning process comprises reading a logical block number for each of the physical blocks by investigating the flash memory based on a latest accessed block.* Paragraph 0052 shows that when the controller reads the data, it compares the counts in fields 43 and 43' of pages having the same LBA and page offset.

x. *And investigating a field of a block allocation table corresponding to the read logical block number.* Figure 9, discussed in paragraph 0049, which is formed from the data in fields 41 and 41', shows the table that provides a mapping from logical blocks to physical blocks.

38. **Claim 8** is taught by Conley as:

y. *The apparatus as claimed in claim 5, wherein the recovery operation recovers from an error by determining a latest accessed physical block for the logical block number among the detected physical blocks according to priorities set during the scanning process, as the valid block.* Conley paragraph 0050 shows that the most recently written page is determined by checking field 43, the timestamp.

z. *And rewriting flash memory state information written in other physical blocks of the detected physical blocks as deleted.* Paragraph 0062 shows that updating one or more blocks of data will result in one or more blocks storing the data to be superceded by the new data, and the blocks with superceded data are identified for erasure.

39. **Claim 9** is taught by Conley and Kim as:

aa. *The apparatus as claimed in claim 5, wherein the recovery operation is performed during the initializing the flash memory.* Kim column 4 lines 22-25 shows that when a flash memory is initially used, a logical unit number to physical unit number table is provided. To generate such a table in a system using the timestamps of Conley, it would be necessary to determine which of the pages sharing the same logical block number and page offset is the most recent page.

40. **Claim 10** is taught by Kim as:

bb. *The apparatus as claimed in claim 5, wherein the recovering from the error is performed during reclaiming the flash memory wherein the reclaiming comprises moving data written in a predetermined unit of the flash memory to a new unit.* Column 8 line 55 to column 9 line 4 teaches that in a reclaim operation, valid blocks and related metadata are copied to a new unit. In order to determine which blocks are valid in a system using the timestamps of Conley, the

timestamps of pages having the same logical block number and page offset must be compared.

41. **Claim 15** is taught by Conley as shown *supra* with respect to claim 11.

42. Although Conley teaches that blocks having the same logical block number can be distinguished by their timestamps, it does not disclose expressly performing a recovery operation.

43. With respect to claim 5, Kim teaches:

cc. *The method as claimed in claim 11, further comprising a recovery operation comprising detecting, during a scanning process, physical blocks for the logical block number and of recovering from an error by determining a valid block for the logical block among the detected physical blocks.* Kim teaches at column 6 lines 29-36 that a recovery operation is required if two valid blocks having the same logical block number exist. In the system disclosed by Conley, paragraph 0050 shows that it can be determined which of multiple pages having the same logical block number and page offset is the correct page by comparing the timestamps of the blocks.

44. At the time of the invention it would have been obvious to one of ordinary skill in the art that a recovery operation is necessary in the event of an error during writing.

45. Conley and Kim are analogous art because they are from the same field of endeavor, the design of flash memory systems.

46. The motivation for doing so would have been to determine which block will be erased during a recovery operation (Kim, column 6 lines 30-36)

47. Therefore, it would have been obvious to combine Kim with Conley for the benefit of determining which pages are old and can be deleted to obtain the invention as specified in **claims 15 and 17**.

48. **Claim 17** is taught by Conley and Kim as:

dd. *The method as claimed in claim 15, wherein the recovering comprises recovering from the error by determining a latest data written among data of a specific logical block number detected during reclaiming the flash memory and wherein the reclaiming comprises moving data written in a predetermined unit of the flash memory to a new unit.* Conley paragraph 0050 shows that the most recently written page is determined by checking field 43, the timestamp. Kim column 8 line 55 to column 9 line 4 teaches that in a reclaim operation, valid blocks and related metadata are copied to a new unit. In order to determine which blocks are valid in a system using the timestamps of Conley, the timestamps of pages having the same logical block number and page offset must be compared.

Allowable Subject Matter

49. **Claims 7 and 16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

50. Applicant's arguments filed 9/20/2007 have been fully considered but they are not persuasive.

51. **First point of Argument**

52. Applicant's arguments with respect to the rejection of claims 2 and 12 under 35 USC 112 first paragraph as failing to comply with the enablement requirement, see the third paragraph beginning on page 8 and continuing on page 9, have been carefully and fully considered, but are not found persuasive. Applicant argues, citing paragraph [51] of the specification:

ee. *"Thus, in the exemplary embodiment of Fig. 4, the memory has two parts, the main area 110, and the spare area. Consequently, a write operation could exist which writes data and meta- information to the main area 110 and the spare area 130, respectively. Thus, Applicant submits one skilled in the art would understand such a write operation could involve writing one value first, e.g., data in the main area 110, and then the second value, e.g., the meta-information in the spare area 130."*

53. The Examiner respectfully notes that an argument that a write could exist does not provide enabling support for the limitations of claims 2, 12, and 20. Paragraph 04-05 of the specification states:

> ff. [04] In such a flash memory, data stored at specific locations can be randomly accessed in the same manner as existing RAMs, nonvolatile storage devices, magnetic devices or the like. **However, when data is modified or deleted, the data is accessed on a block basis contrary to existing storage devices**.
>
> gg. [05] That is, in the flash memory, **access is gained based on the block which written data is retrieved from or data is written in at once during read/write operations**, and based on a unit which comprises a plurality of blocks and can be erased through one delete operation. As a method of efficiently managing data according to the access characteristics of the flash memory, a block (of sector) re-mapping scheme has been generally used.

54. The Examiner maintains that this section shows that the basic write unit in the flash memory disclosed in the specification of the instant application is called a block. Paragraph 51 states that the main area 110 and the spare area 130 are part of the same block. Accordingly, it would require the ability to perform a write smaller than what is disclosed to be the write unit to perform the limitations of claims 2, 12, and 20.

55. **Second point of Argument**

56. Applicant's arguments with respect to the rejection of claims 1, 3-4, 11, and 13-14 under 35 USC 102(b) as being anticipated by Conley, see the second paragraph

beginning on page 9 through the second paragraph beginning on page 11, have been carefully and fully considered, but is not found persuasive.

57. Applicant's arguments with respect to claim 1's requirement that flash memory state information is written in a previous physical block, see the first and second paragraphs beginning on page 10, are found persuasive. However, this is not sufficient to overcome the rejection of claims 1, 3-4, 11, 13-14, 18-19, and 21.

58. Applicant argues in the first and second paragraphs beginning on page 11:

hh. "Moreover, as noted previously, Conley merely discloses a physical block having a logical block number and a time stamp. The time stamp used in Conley simply indicates the time data was last written to the physical block. A time stamp is different from state information since a time stamp indicates time, whereas state information indicates a status.

ii. *Further, Conley fails to discuss state information, i.e., a status of the physical block itself. Since the claimed invention requires, inter alia, flash memory state information written in a previous physical block, Applicant submits Conley does not teach or suggest the feature "without changing flash memory state information written in a previous physical block," as claimed."*

59. The Examiner respectfully disagrees. Conley teaches the use of field 43 to determine if a page contains new or old data, see paragraph 0052. Accordingly, the time stamp of Conley is not used just to show when the page was written, but is used to determine which of a plurality of physical pages having the same logical address contain valid data. Accordingly, field 43 is used by the system of Conley to determine if

the page is valid or invalid (identified as new or superceded in paragraph 0052). Accordingly, field 43 indicates to the system if a given page of data is valid, and therefore indicates the state (or status) of the page.

60. Additionally, the Examiner respectfully points out that field 43 is not limited to being a timestamp. Paragraph 0051 of Conley teaches that instead of a timestamp, the output of modulo-N counter may be used as the value of field 43. Specifically, paragraph 0051 states:

> jj. "*One specific technique is to store the output of a modulo-N counter as the value of the field 43. The range of the counter should be one more than the number of pages that are contemplated to be stored with the same logical page number. When updating the data of a particular page in the original block PBN0, for example, the controller first reads the count stored in the field 43 of the page whose data are being updated, increments the count by some amount, such as one, and then writes that incremented count in the new block PBN1 as the field 43'.*"

Conclusion

61. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Examiner
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DONALD SPARKS
SUPERVISORY PATENT EXAMINER